ZJW AF 2188

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. PHN17,438

In Re Application Of: **Louis M. Meli**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/313,037	05/17/1999	Paul A. Baker	24737	2188	3381

Invention:

DATA PROCESSING DEVICE WITH ALIASED DATA POINTER REGISTER

COMMISSIONER FOR PATENTS:

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Dated: **March 23, 2005**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Meli

Art Unit: 2188

Serial No.: 09/313,037

Examiner: Baker, Paul

Filed: 5/17/99

Attorney Docket No.: PHN-17,438

Title: DATA PROCESSING DEVICE WITH ALIASED DATA POINTER REGISTER

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BRIEF OF APPELLANTS

This is an appeal from the Final Rejection dated November 12, 2004, rejecting claims 1-10. This Brief is accompanied by the requisite fee set forth in 37 C.F.R. §1.17 (c).

REAL PARTY IN INTEREST

U.S. Philips Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

As filed, this case included claims 1-10. Claims 1-10, stand rejected, and form the basis of this appeal. No claims have been allowed.

STATUS OF AMENDMENTS

No After-Final Amendment was filed.

SUMMARY OF THE INVENTION

The present invention provides a data processing device, having: (1) a register circuit for storing at least two addresses in parallel; (2) an address selector arranged to cycle through a set of states in which respective ones of the at least two addresses become a currently selected address respectively; (3) an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states; and (4) a control register that is instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction.

Accordingly, the present invention provides a device that can cause an address selector to cycle through states to alternate among parallel stored addresses in response to a memory access signal; and selectively cause "updates" (e.g., increment, decrement) to the

addresses as dictated by a control register.

ISSUES

1. Whether claims 1-10 are unpatentable under 35 U.S.C. §103(a) as over Pawloski (U.S. Patent No. 5,426,769), hereafter "Pawloski" in view of Dallas Semiconductor "DS87C550 Product Preview," hereafter "Dallas."

GROUPING OF CLAIMS

Claims 1-10 stand or fall together.

ARGUMENT

In the Office Action, claims 1-10 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Pawloski (U.S. Patent No. 5,426,769), hereafter "Pawloski" in view of Dallas Semiconductor "DS87C550 Product Preview," hereafter "Dallas."

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the

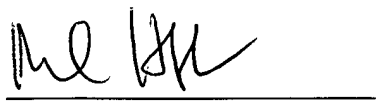
claim limitations. Appellant respectfully submits that the Pawloski and Dallas references, taken alone or in combination, fail to meet each of the three basic criteria required to establish a *prima facie* case of obviousness. As such, the rejection under 35 U.S.C. 103(a) is defective.

Appellants initially submit that the cited combination fails to teach or suggest each of the claim limitations. For example, with respect to independent claim 1 (and similarly 10), Appellant claims a data processing device having "a register circuit for storing at least two addresses in ***parallel***." In the final Office Action, the Examiner alleges that Dallas teaches the feature of at least two "addresses" stored in parallel, namely DPRT0 and DPTR1, as shown in Figure 1 of Dallas. It is initially noted that Figure 1 of Dallas does not show DPTR1, and that Appellant claims a ***circuit*** for storing addresses in parallel, not merely parallel addresses. Nonetheless, as clearly described in Dallas on page 14, DPRT0 and DPTR1 consist of non-parallel registers located within an integrated circuit chip. Namely, Dallas states that "DPTR1 is located at the next two register locations (up from DPTR0)." Accordingly, Dallas fails to disclose "a register circuit for storing at least two addresses in *parallel*." Instead, Dallas discloses "sequential" register addresses that are physically and logically addressed at two different locations. (Appellant notes that the SFR's taught by Pawloski are likewise non-parallel based on the same reasoning.) In contrast, Appellant's invention discloses a structure, i.e., circuit, for storing addresses in parallel (see, e.g., Appellant's Figures 1 and 2). Accordingly, Appellant submits that because the cited art fails to teach or suggest a register circuit for storing at least two addresses in parallel, the obviousness rejection should be withdrawn.

Appellants further submit that there would be no reasonable expectation of success when combining the references, as suggested by the Examiner. As noted above, the Examiner (incorrectly) alleges that Dallas teaches at least two "addresses" stored in parallel, namely DPRT0 and DPTR1. The Examiner further alleges that the control SFR of Pawloski teaches the feature of "a control register that controls whether or not the processing device updates the at least two addresses as a side-effect of executing a memory access instruction." As is evident, Pawloski teaches an ***external*** decoder and memory space that includes a control special function register SFR that can be programmed to enable and disable auto-incrementing. However, in order to properly combine the two references, the control SFR of Pawloski must be capable of controlling the updating of "the at least two addresses." That is, the control SFR, which resides on an external device, must be able to update the ***internal*** DPRT0 and DPTR1 registers taught in Dallas. In order to achieve this, a structure would be needed to externally access the internal behavior of the DPRT0 and DPTR1 registers. No such functionality is taught or suggested by either reference. Thus, the functions performed by the control register as recited in the present invention are not equivalent to the control SFR in Pawloski. Accordingly, Appellant submits that there would be no reasonable expectation of success for combining the references, and as such, respectfully requests that the rejection be withdrawn.

Appellant submits that all dependant claims are allowable for the reasons stated above, as well as for their own distinct features. In light of the above, Appellant submits that claims 1-10 are allowable and respectfully requests reversal of the final rejection.

Respectfully submitted,



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APPENDIX

Claim listing

1. A data processing device, comprising

a register circuit for storing at least two addresses in parallel;

an address selector arranged to cycle through a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states; and

a control register that is instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction.

2. The data processing device as claimed in claim 1, wherein each control state specifies respective update actions for all of the at least two addresses.

3. The data processing device as claimed in claim 1, wherein the control states specify a choice from at least no-update, update by incrementing with a predetermined value and update by decrementing with the predetermined value.

4. The data processing device as claimed in claim 1, wherein the execution of said memory access instruction further causes the instruction execution unit to perform, upon the currently selected address, the update action that is specified by the control state of the control register for that one of the at least two addresses that is the currently selected address.

5. The data processing device as claimed in claim 1, wherein the instruction set includes a load from memory instruction and a store to memory instruction for causing the instruction execution unit to respond to the execution of said memory access instruction.

6. A data processing system comprising a data processing device as claimed in claim 5, programmed with a program for executing alternately the load from memory instruction and the store to memory instruction, for an address addressed by a first one and a second one of the at least two addresses respectively, after setting the control register to one of control states that causes both the first one and the second one of the addresses to be updated.

7. A data processing system comprising a data processing device as claimed in claim 5, programmed with a program for executing alternately the load from memory instruction and the store to memory instruction, for an address addressed by a first one and a second one of the at least two addresses respectively, after setting the control register to one of control states that causes only one of the first or second one of the addresses to be updated.

8. The data processing device as claimed in claim 1, wherein the address selector cycles back and forth between states that select a first and second one of the at least two addresses respectively.

9. The data processing device as claimed in claim 1, wherein the register circuit stores at least three addresses, and the address selector cycles through a series of at least three states that select different ones of the at least two addresses.

10. A data processing device, comprising

a register circuit for storing at least two addresses in parallel;

an address selector including a register selector register and a logic circuit collectively arranged to cycle through a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access sigmals with an access address determined from the currently

selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states; and

a control register in communication with said register selector register and said logic circuit, said control register being instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction.